CLAIMS

1. A semiconductor package provided with:

an interconnection layer including an interconnection pattern and pad formed on an insulating substrate or insulating layer,

a protective layer covering said interconnection layer except at the portion of said pad and said insulating substrate or insulating layer, and

an external connection terminal bonded with said pad exposed from said protective layer,

the pad to which the external connection terminal is bonded being comprised of a plurality of pad segments,

sufficient space being opened for passing an interconnection between pad segments, and

the pad segments being comprised of at least one pad segment connected to an interconnection and other pad segments not connected to interconnections.

2. A semiconductor package as set forth in claim 1, wherein each of said external connection terminals is assigned for signal use, power use, or ground use and an interconnection for signal use is passed between the plurality of pad segments forming a pad to which an external connection terminal assigned for ground use is connected.

3. A semiconductor package as set forth in claim 2, where said ground use interconnection surrounds said signal use interconnection at a lower layer.

4. A semiconductor package as set forth in claim 1, wherein each of said external connection terminals is assigned for signal use, power use, or ground use and an interconnection for power use is passed between the plurality of pad segments forming a pad to which an external connection terminal assigned for ground use is connected.

5. A semiconductor package as set forth in claim 1, wherein a width of said interconnections is 30 μm and

a space sufficient for passing said interconnection is 150 μm.

6. A process of producing a semiconductor package comprising the steps of:

forming a plurality of pad segments forming each pad to which each external connection terminal is bonded while opening up spaces sufficient for passing interconnections therebetween when forming an interconnection layer including interconnection patterns and pads on an insulating substrate or insulating layer,

forming a protective layer covering said interconnection layer other than at portions of pads formed by said plurality of pad segments and said insulating substrate or insulating layer, and

bonding one external connection terminal to each pad formed by said plurality of pad segments exposed from said protective layer.

7. A process of producing a semiconductor module as set forth in claim 6, further comprising the steps of:

forming a protective film and

forming a plating film for improving adhesion when bonding the external connection terminals to the pad segments exposed from said protective film.

8. A semiconductor module comprised of a semiconductor package of any one of claims 1 to 5 and a semiconductor chip mounted on a surface of the package opposite to the surface where external connection terminals are bonded so that the electrode terminals of said semiconductor chip are electrically connected to said interconnection layer.